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Design and FPGA Synthesis of Three Stage Telecommunication Switching in HDL Environment

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Abstract

Telecommunication networks are based on crossbar switching structure. Non-blocking crossbar switching structure is used crosspoint switch fabric ICs. High performance non-blocking matrixes cross point switches are use to avoid the congested path to the output, and eliminate the bandwidth problem of one at a time. Telecommunication switching uses multistage crossbar switching to overcome the limitations of individual chips or boards. The research paper focuses on the FPGA implementation of 64 x 64 three stage telecommunication switching. The generic architecture scheme is followed to implement 64 x 64 three stage network configuration, with 64 inlets and 64 outlets as cluster size. The design is developed with the help of Xilinx ISE 14.2, software, synthesized on Virtex- 5 FPGA, and function simulation is carried out in Modelsim 10.1b student edition. Very High Speed Integrated Circuit Hardware Description Language (VHDL) is used to develop the design.

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Keywords: Very Large Scale of Integration (VLSI), Field Programmable Gate Array (FPGA), Hardware Description Language (HDL), Stored Program Control (SPC), Staged Networks

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1. Introduction

Stored program control (SPC) concept is used by modern digital computers. In SPC[5], a set of instructions or program is stored in its memory and processor is executing the instructions one by one automatically. All the control functions of the exchange are executed through programs stored in the memory, that's what the nomenclature is, stored program control. A telephone exchange[3] is operating 24 hours in a day, 365 days and numbers of years without interruption[9]. It means that the exchange should be highly tolerant to control the faults. Today, all exchanges are based on the SPC, which is an attempt to replace the space division electromechanical switching matrices by semiconductor cross point matrices. Speed, size and cost are three important factors while designing the electronic system. Microprocessor/microcontroller (MPMC) [5,9] system can handle sequential operations with high flexibility and use of Field Programmable Gate Array (FPGA) can handle concurrent operations with high speed in small size area. So system performance can be enhanced with the combination of these features. The combination of SPC and its implementation in Hardware Description Language (HDL) environment leads to Programmable Telephone Switching System (PTSS), which can be designed using combination of stored program control (SPC) and VLSI technology. In traditional Telephone switching systems[7], it is not possible to increase the junction or extension lines[7] because of limitation of processor or controlling system. If it is tried to design the system with higher processors then it became cost effective and complicated. Solution for this problem is to implement the controlling system for couple of lines in FPGA and make provision to co-control [15] or cascade to the other FPGA of another line so that many lines are possible.

In the staged network an inlet is connected directly to an outlet through the single crosspoint. In single stage network each individual cross point can be used to connect to inlet and outlet pair. So, the possible number of inlet and outlet pairs is equal to N (N-1)/2 in a triangular array [9] and N (N-1) for a square array. For a large single stage network, the number of crosspoint switches is prohibitive and a specific crosspoint is needed for specific connection. The data is mostly circulated a number of times in the network, if source subscriber want to establish a connection with destination subscriber. The major problem in the single stage network is that any crosspoint failure can cause no data transfer to the destination or connection establishment to the destination is not possible, there is not any alternate path. The association of large numbers of crosspoints on inlets and outlets leads to capacitive loading on the message path. For a single stage larger exchange crosspoints are very insufficiently utilized. For example in a square switch, only one crosspoint is used in each column or row, but all lines are active. To enhance the switching capacity and efficiency of telephone exchange, it is necessary that any crosspoint be usable for more than one potential connection. If there are more than one paths or alternate paths available for any connection, however, crosspoints[7] are to be shared so that blocking will not occur. Alternate paths reduce the blocking probability and also protect the exchange to be failure. Intact, single stage networks suffer with many disadvantages, sharing of crosspoints for alternate paths through the switch can be overcome by considering the concept of multistage switching networks.

2. Three Stage Network

The real advantage of multistage switching[6,9] is realized when the network is realized in three or more stages. Considering a three stage $N \times N$ network as shown in fig. 1, in which N inlets are divided into a blocks having x inlets ($N = a \times x$) and N outlets are also divided into a blocks having x outlets ($N = a \times x$). The three stage network is realized switching matrices of size $x \times b$ in first stage, $a \times a$ in second stage and $b \times x$ in third stage. Network has b alternative paths to reach any outlet of third stage. The total number of crosspoints can be calculated

$$S = a\ x\ b + ba^2 + bxa \qquad (4)$$

$$S = 2\ a\ x\ b + ba^2 \qquad (5)$$

Putting the value of ($N = a \times x$) in the equation, the number of cross points are given as

$$S = b(\ 2N + a^2) \qquad (6)$$

The switching capacity of three stage network can be calculated, when the network is fully available.

$$Switching\ capacity = aba = a^2b \qquad (7)$$

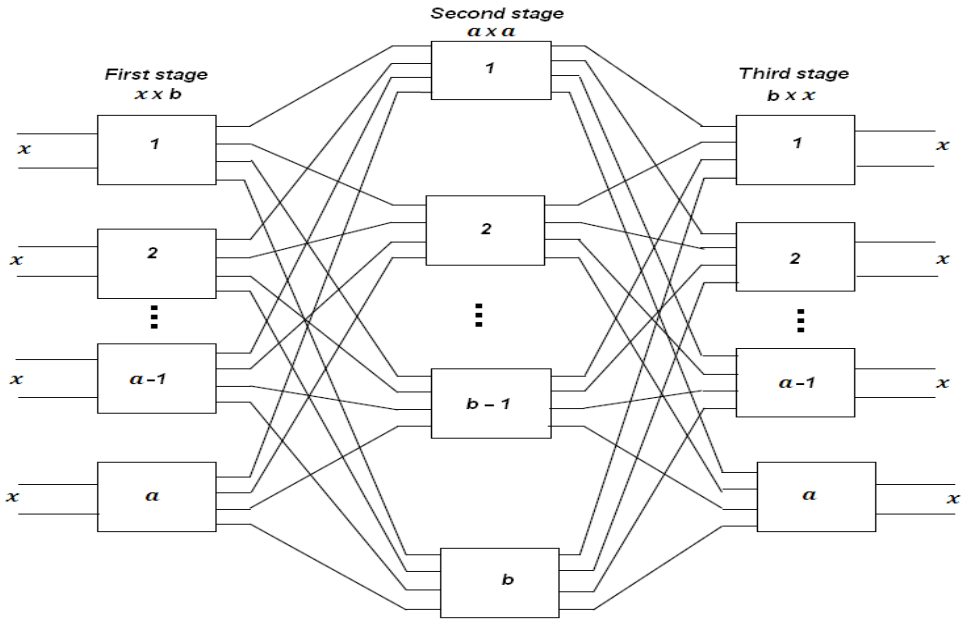

Fig. 1 Three stage switching [9]

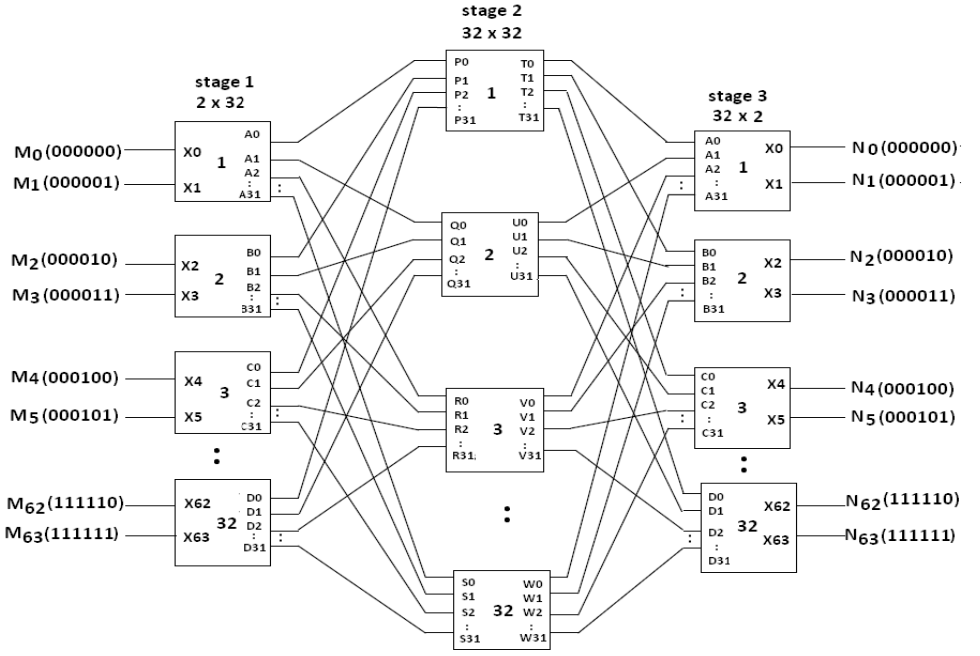

Fig. 2 Three stage swtching and routing (64 x 64)

In the 64 × 64 three stage networks shown in fig. 2, $Switching\ capacity = a^2b = 32^2 \times 32 = 32768$. It means, three stage (64 × 64) network is capable to support 32768 calls simultaneously. The number of crosspoints, for three stage (64 × 64) network is calculated using equation (5).The number of crosspoints$S = 2\ a\ x\ b + ba^2 = 2 \times 32 \times 2 \times 32 + 32 \times 32^2 = 4096 + 32768 = 36864$. The routing scheme of the network can be understood with the help of table 1. Suppose user $M_0\ (000000)$ want to communicate $N_0(000000)$, then there are 32 alternative

paths. The exists paths are M0(000000) → X_0→ A_0 → P_0 →T_0 →A_0→ X_0 → N_0(000000), M_0(000000) →X_0 → A_1→ Q_0→U_0 →A_1→X_0 → N_0(000000), M_0(000000) →X_0 → A_2→ R_0→ V_0 →A_2→ X_0 → N_0(000000)…….. M_0 (000000) →X_0 → A_{31}→ S_0→ W_0 →A_{31}→ X_0 → N_0(000000). Similarly all the subscribers are having 32 alternative paths. The advantage of three stage multistage network is that, if any path in the network is busy, there are also alternative paths to route the calls.

Table 1 Routing scheme of three stage network (64 x 64)

Inlet Address	Outlet Address	Routing
M_0 (000000)	N_0(000000)	M_0(000000) → X_0→ A_0 → P_0 →T_0 →A_0→ X_0 → N_0(000000) M_0(000000) →X_0 → A_1→ Q_0→U_0 →A_1→X_0 → N_0(000000) M_0(000000) →X_0 → A_2→ R_0→ V_0 →A_2→ X_0 → N_0(000000) : : M_0(000000) →X_0 → A_{31}→ S_0→ W_0 →A_{31}→ X_0 → N_0(000000)
	N_1(000001)	M_0 (000000)→X_1 → A_0→ P_0→T_0 →A_0→ X_1 → N_1(000001) M_0 (000000)→X_1 → A_1→ Q_0→U_0 →A_1→X_1 → N_1(000001) M_0(000000) →X_1 → A_2→ R_0→ V_0 →A_2→ X_1 → N_1(000000) : : M_0(000000) →X_1 → A_{31}→ S_0→ W_0 →A_{31}→ X_1 → N_1(000001)
	N_2(000010)	M_0(000000) →X_2 → B_0→ P_1→T_1 →B_0→ X_2 → N_2(000010) M_0(000000) →X_2 → B_1→ Q_1→U_1 →B_1→ X_2 → N_2(000010) M_0(000000) →X_2 → B_2→ R_1→V_1 →B_2→ X_2 → N_2(000010) : : M_0(000000) →X_2 → B_{31}→ S_1→ W_1 →B_{31}→ X_2 → N_2(000010)
	N_3(000011)	M_0(000000) →X_3 → B_0→ P_1→T_1 →B_0→ X_3 → N_3(000011) M_0(000000) →X_3 → B_1→ Q_1→U_1 →B_1→ X_3 → N_3(000011) M_0(000000) →X_3→ B_2→ R_1→ V_1 →B_2→ X_3 → N_3(000011) : : M_0(000000) →X_3 → B_{31}→ S_1→ W_1→B_{31}→ X_3 → N_3(000011)
	N_4(000100)	M_0(000000) →X_4 → C_0→ P_2→T_2 →C_0→ X_4 → N_4(000100) M_0(000000) →X_4 → C_1→ Q_2→U_2 →C_1→ X_4 → N_4(000100) M_0(000000) →X_4 → C_2→ R_2→ V_2 →C_2→ X_4 → N_4(000100) : : M_0(000000) →X_4 → C_{31}→ S_2→ W_2 →C_{31}→ X_4 → N_4(000100)
	: :	: :
	N_{62}(111110)	M_0(000000) →X_{62} → D_0→ P_{31}→T_{31} →D_0→ X_{62} → N_{62}(111110) M_0(000000) →X_{62} → D_1→ Q_{31}→U_{31} → D_1→ X_{62} → N_{62}(111110) M_0(000000) →X_{62} → D_2→ R_{31}→ V_{31} → D_2→ X_{62} → N_{62}(111110) : : M_0(000000)→X_{62} → D_{31}→ S_{31}→ W_{31} → D_{31}→ X_{62} → N_6(111110)
	N_{63}(111111)	M_0(000000) →X_{63} → D_0→ P_{31}→T_{31} →D_0→ X_{63} → N_{63}(111111) M_0(000000) →X_{63} → D_1→ Q_{31}→U_{31} → D_1→ X_{63} → N_{63}(111111) M_0(000000) →X_{63} → D_2→ R_{31}→ V_{31} → D_2→ X_{63} → N_{63}(111111) : : M_0(000000)→X_{63}→ D_{31}→ S_{31}→ W_{31} → D_{31}→ X_{63} → N_{63}(111111)
:	:	:
:	:	:
:	:	:
M_{63}(111111)	N_{63}(111111)	M_{63}(111111) →X_{63} → D_0→ P_{31}→T_{31} →D_0→ X_{63} → N_{63}(111111) M_{63}(111111) →X_{63} → D_1→ Q_{31}→U_{31} → D_1→ X_{63} → N_{63}(111111) M_{63}(111111) →X_{63} → D_2→ R_{31}→ V_{31}→ D_2→ X_{63} → N_{63}(111111) : : M_{63}(111111)→X_{63}→D_{31}→ S_{31}→ W_{31} → D_{31}→ X_{63} → N_{63}(111111)

3. Results & Discussions

The snapshot is taken from the modelsim 10.1b software which shows the 8 bit data transfer among inlets and outlets. In the snapshot of modelsim simulation, inlets are represented with M_0 [7:0], M_1[7:0]…… M_{62} [7:0] and M_{63}[7:0] carrying 8 bit data. Outlets N_0[7:0], N_1[7:0]…… N_{62}[7:0] and N_{63}[7:0] carrying 8 bit data also carrying 8 bit data. *in_node_address[5:0]* and *out_node_address[5:0]* are the addresses of inlets and outlets. *write_en* and *read_en* are the control signals considered for data writing in intermediate stages and reading out to appropriate outlets. The functional simulation depends on the test inputs in design. c*lk* and *reset* are used for the synchronization.

Step input 1: reset = '1', clk is used for synchronization and then run.

Step input 2: reset = '0', same clk is used for synchronization. Select the address of destination node, out_node_address. Force the eight bit value to any inlet.

Step input 3: write_en = '0' and read_en = '1 and run. Desired output on corresponding outlet is achieved.

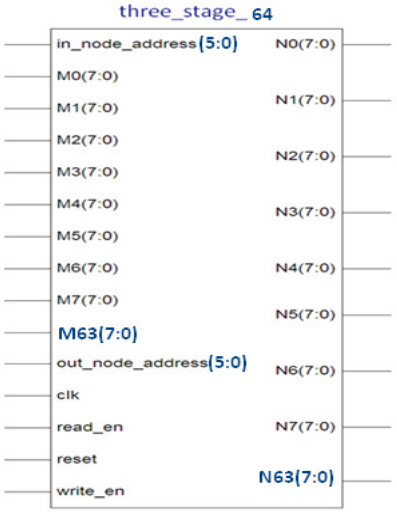

Fig. 3 RTL view of three stage (64 x 64) network

Register Transfer Logic (RTL) view can be viewed in ISE 14.2 Xilinx HDL environment, is shown in fig. 3. The snapshot of the RTL view is shown in the fig. 4, for three stages (64 × 64) network. Table 2 shows the design pins and their functionality used to design stage the three stage network.

Table 2 Design pins and their functional description

Pins	Functional Description
reset	Used for synchronization of the components by using clk
clk	Default input for sequential logic to work on rising edge of clock pulse.
in_node_address [5:0]	Address of source subscribers or inlets
out_node_address [5:0]	Address of destination subscribers or outlets
M_0 [7:0]	Inlet with in_node_address = 000000 carrying 8 bit data
M_1 [7:0]	Inlet with in_node_address = 000001 carrying 8 bit data
M_2 [7:0]	Inlet with in_node_address = 000010 carrying 8 bit data
:	:
M_{63} [7:0]	Inlet with in_node_address = 111111 carrying 8 bit data
N_0 [7:0]	Outlet with out_node_address = 000000 receiving 8 bit data
N_1 [7:0]	Outlet with out_node_address = 000001 receiving 8 bit data
:	:
N_{63} [7:0]	Outlet with out_node_address = 111111 receiving 8 bit data

data_in[7:0]	Represents input data of 8 bits
data_out[7:0]	Represents input data of 8 bits
read_en	control signal to read data from memory
write_en	control signal to write data in memory

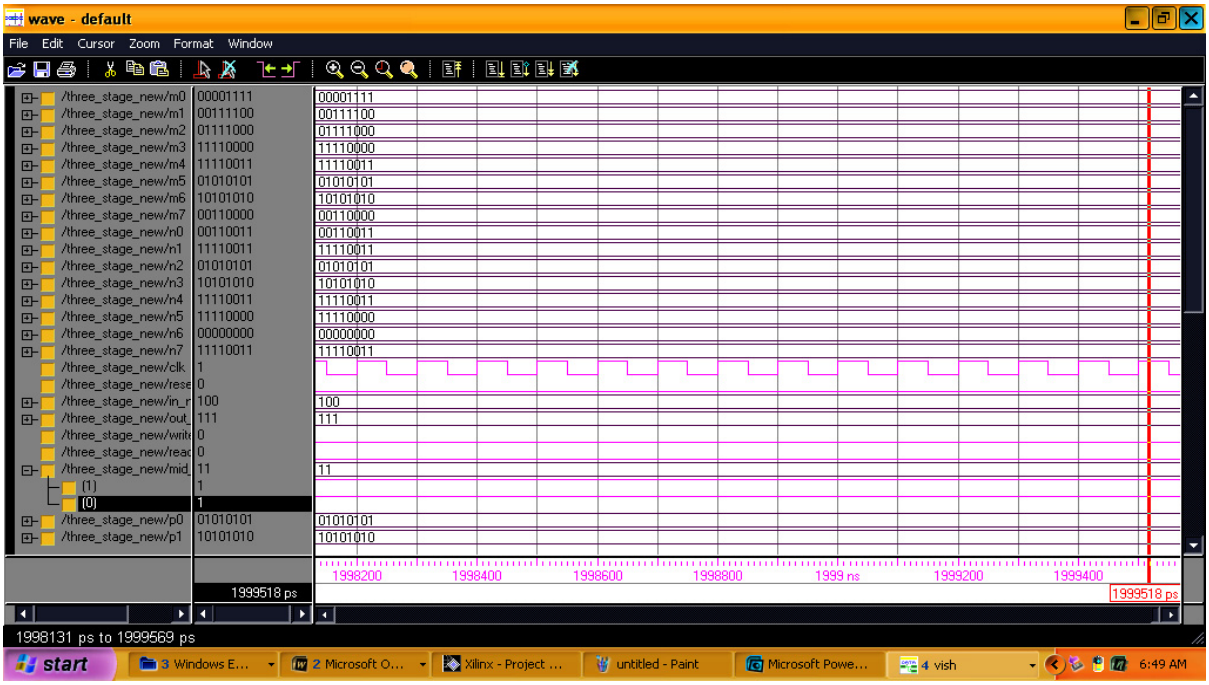

Fig. 4 Modelsim waveform of three stage switching (64 x 64)

4. Device Utilization and Timing Summary

Device utilization summary is the report of used device hardware in the implementation of the chip such as RAM, ROM, slices, flip flops etc. The synthesis report shows the complete details of device utilization. If the designed chip is not having the optimized hardware parameters, further chip development is done in the Xilinx ISE design software. Table 3 shows the hardware utilization for the staged structure. Target Device: xc5vlx20t-2-ff323, Virtex 5, is the device targeted for FPGA. Timing details provides the information of delay, minimum period, minimum input arrival time before clock and maximum output required time after clock. Table 4 lists the details of minimum period, maximum frequency, minimum input arrival time before clock, maximum output required time after clock and memory utilization for three stage network.

Table 3 Utilization in three stage network (64 × 64)

Device utilization			Timing details	
Device Part	Utilization		Timing Parameter	Utilization
Number of slices	128 out of 12480	1%	**Minimum period**	1.309ns
Number of slice flip flops	189 out of 12480	1%	**Maximum frequency**	400.00 MHz
Number of 4 input LUTs	128 out of 189	67%	**Minimum input arrival time before clock**	2.902ns
Number of bonded IOBs	138 out of 172	80 %	**Maximum output required time after clock**	2.830ns
Number of GCLKs	1 out of 32	3%	**Total memory usage**	173004 kB

5. Conclusions

The hardware chip implementation of three stages multistage telecommunication network is done in hardware description language environment. The results are validated on the FPGA kit of Digilent manufactured Virtex-5. The chip implementation is done for a cluster configuration (64 × 64) as inlets and outlets. FPGA designing of switching system tried to make the whole switching system programmable to increase the performance, reduce the traffic congestion, and reduction in the delay. The research work is a significant effort towards total digitization and programmable of switching systems and would surely prove a boon for VLSI design industry. An additional research can be done with adding features of security by encryption and decryption of data transfer among inlets and outlets. In future the chip implementation can be done for four stages, five stages switching and more number of stages with variable number of inlets and outlets.

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